We claim:

1. An IC test apparatus comprising:

a. a rigid support member having an opening therein, thereby defining a peripheral edge around the opening,

b. a polymer membrane attached to the rigid support member and having a center portion covering the opening,

c. a probe contact array on the center portion of the polymer membrane,

d. a wafer platform,

e. means for depressing the center portion of the polymer membrane toward the wafer platform,

f. at least one reference IC chip located adjacent to the peripheral edge of the opening in the rigid support,

g. interconnection means interconnecting the reference IC chip and the probe contact array.

2. The apparatus of claim 1 wherein the reference IC chip includes at least one LC circuit.

3. The apparatus of claim 1 wherein the opening has four sides, the apparatus further comprising a first reference IC chip located adjacent one side and a second IC reference chip located adjacent another side.

4. The apparatus of claim 1 further including at least one reference component attached to the polymer membrane adjacent to the probe contact array.

5. The apparatus of claim 4 wherein the reference component comprises an LC circuit.

6. An IC test apparatus comprising:

a. a rigid support member having an opening therein, thereby defining a peripheral edge around the opening,

b. a polymer membrane attached to the rigid support member and having a center portion covering the opening,

c. a probe contact array on the center portion of the polymer membrane,

d. a wafer platform,

e. means for depressing the center portion of the polymer membrane toward the wafer platform,

f. at least one reference component attached to the polymer membrane and located adjacent to the probe contact array, and

g. interconnection means interconnecting the reference component and the probe contact array.

7. The apparatus of claim 6 wherein the reference component comprises an LC circuit.

8. The apparatus of claim 7 wherein the reference component is part of a passive IC chip.

9. The apparatus of claim 6 wherein the reference component is part of a digital test circuit.

10. An IC test apparatus comprising:

a. a rigid support member having an opening therein, thereby defining a peripheral edge around the opening,

b. a polymer membrane attached to the rigid support member and having a center portion covering the opening,

c. a probe contact array on the center portion of the polymer membrane,

d. a wafer platform,

e. means for depressing the center portion of the polymer membrane toward the wafer platform,

f. a reference IC chip attached to the polymer membrane and located adjacent to the probe contact array, and

g. interconnection means interconnecting the reference component

and the probe contact array.

11. The apparatus of claim 10 wherein the reference IC chip comprises a passive IC chip.

12. The apparatus of claim 10 wherein the reference IC chip comprises an active IC chip.

13. A method for testing an IC wafer comprising:

a. mounting a probe membrane on a rigid support member, the rigid support member having an opening therein, and the probe membrane attached to the rigid support member with a center portion thereof covering the opening, the center portion including a probe contact array, and a reference component,

b. mounting a wafer under test on a platform under the opening,

c. moving the center portion of the probe membrane so that the probe contact array comes into contact with the wafer under test, and

d. passing electrical test signals between I/Os on the wafer under test and a test circuit.

14. The method of claim 13 further including the step of matching the impedance of the I/Os on the wafer with the reference component.

15. The method of claim 14 wherein the reference component is part of an IC chip located on the probe membrane.

16. The method of claim 14 wherein the wafer under test comprises IC chips with analog components and the reference component includes one or more capacitors and inductors.

17. A method for testing an IC wafer comprising:

a. mounting a probe membrane on a rigid support member, the rigid support member having an opening therein, and the probe membrane attached to the rigid support member with a center portion thereof covering the opening, the center portion including a probe contact array, and a reference IC,

b. mounting a wafer under test on a platform under the opening,

c. moving the center portion of the probe membrane so that the probe contact array comes into contact with the wafer under test, and

d. passing electrical test signals between I/Os on the wafer under test and a test circuit.

18. The method of claim 17 wherein the I/Os on the wafer under test and the reference IC comprise a fully functional system.

19. A method for testing an IC wafer, the wafer comprising analog IC chips adapted for operation at frequencies above 1 GHz, the method comprising:

a. probing the analog IC chips with an array of test contacts, and

b. performing a fully functional test of the analog functions of the analog IC chips.